Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A method of programming an electrically programmable memory, the method comprising:

accessing a group of memory cells of an electrically programmable memory to ascertain a programming state thereof;

applying a programming pulse to those memory cells in the group whose programming state is not ascertained to correspond to a desired programming state; and

repeating the steps of accessing and applying for the memory cells in the group whose programming state is not ascertained to correspond to a desired programming state, wherein

after the programming state of a prescribed number of memory cells in the group has been ascertained to correspond to a desired programming state, accessing again the memory cells in the group and re-ascertaining the programming state of the memory cells whose programming state was previously ascertained to correspond to a desired programming state; and

applying at least one additional programming pulse to those memory cells in the group whose programming state is not re-ascertained to correspond to a desired programming state.

2. (Original) The method according to claim 1, wherein the electrically programmable memory comprises at least one memory of type of at least one of EPROM, EEPROM, and Flash memory.

3. (Original) The method according to claim 1, in which the act of re-ascertaining is performed after the programming state of all the memory cells in the group has been ascertained to correspond to a desired programming state.

4. (Original) The method according to claim 1, in which the applying a programming pulse comprises varying, substantially at each programming pulse, a voltage applied to a control electrode of the memory cells of the group, progressively passing from a first voltage to a second voltage.

5. (Original) The method according to claim 4, in which the applying at least one additional programming pulse comprises restarting from the voltage applied to a control electrode of the memory cells equal to the first voltage.

6. (Original) The method according to claim 4, in which the applying at least one additional programming pulse comprises restarting from a voltage applied to a control electrode of the memory cells intermediate between the first voltage and the second voltage.

7. (Original) The method according to claim 6, comprising establishing a programming voltage value for which the programming state of at least one of the memory cells in the group is ascertained first to correspond to a desired programming state, and determining the intermediate voltage on the basis of the established programming voltage value.

8. (Original) The method according to claim 4, in which the varying comprises progressively increasing the voltage applied to the control electrode of the memory cells from a lower value to a higher value.

9. (Original) The method according to claim 1, further comprising, after the act of applying at least one additional programming pulse, accessing again the memory cells in the group for ascertaining the programming state of the memory cells whose programming state was previously not re-ascertained to correspond to a desired programming state.

10. (Original) The method according to claim 9, in which the act of re-ascertaining is performed after the programming state of all the memory cells in the group has been ascertained to correspond to a desired programming state.

11. (Original) The method according to claim 9, in which the applying a programming pulse comprises varying, substantially at each programming pulse, a voltage applied to a control electrode of the memory cells of the group, progressively passing from a first voltage to a second voltage.

12. (Original) The method according to claim 11, in which the applying at least one additional programming pulse comprises restarting from the voltage applied to a control electrode of the memory cells equal to the first voltage.

13. (Original) The method according to claim 11, in which the applying at least one additional programming pulse comprises restarting from a voltage applied to a control electrode of the memory cells intermediate between the first voltage and the second voltage.

14. (Original) The method according to claim 13, comprising establishing a programming voltage value for which the programming state of at least one of the memory cells in the group is ascertained first to correspond to a desired programming state, and determining the intermediate voltage on the basis of the established programming voltage value.

15. (Original) The method according to claim 11, wherein the varying comprises progressively increasing the voltage applied to the control electrode of the memory cells from a lower value to a higher value.

16. (Currently Amended) A circuit for programming memory cells of an electrically programmable memory, comprising:

a circuit for applying programming pulses to groups of memory cells of an electrically programmable memory;

a circuit for accessing the memory cells in the group and ascertaining a programming state thereof; and

a control circuit for controlling the circuit for applying programming pulses so that programming pulses are repeatedly applied to the memory cells in the group until the programming state thereof is ~~not~~ ascertained to correspond to a desired programming state, wherein

the control circuit causes the circuit for accessing and ascertaining to access the memory cells in the group and re-ascertain the programming state of the memory cells whose programming state was previously ascertained to correspond to a desired programming state after the programming state of a prescribed number of memory cells in the group has been ascertained to correspond to a desired programming state, and in that

the control circuit causes the circuit for applying programming pulses to apply at least one additional programming pulse to those memory cells in the group whose programming state is not re-ascertained to correspond to a desired programming state.

17. (Original) The circuit of claim 16, wherein the electrically programmable memory comprises at least one memory of type of at least one of EPROM, EEPROM, and Flash memory.

18. (Currently Amended) An integrated circuit comprising:

a circuit supporting substrate;

at least one electrically programmable semiconductor memory being at least partially supported by the circuit supporting substrate; and

a circuit for programming memory cells of the at least one electrically programmable semiconductor memory, the circuit being electrically coupled with the at least one electrically programmable semiconductor memory and further being at least partially supported by the circuit supporting substrate, the circuit comprising:

a circuit for applying programming pulses to groups of memory cells of the at least one electrically programmable semiconductor memory;

a circuit for accessing the memory cells in the group and ascertaining a programming state thereof; and

a control circuit for controlling the circuit for applying programming pulses so that programming pulses are repeatedly applied to the memory cells in the group until the programming state thereof is ~~not~~ ascertained to correspond to a desired programming state, wherein

the control circuit causes the circuit for accessing and ascertaining to access the memory cells in the group and re-ascertain the programming state of the memory cells whose programming state was previously ascertained to correspond to a desired programming state after the programming state of a prescribed number of memory cells in the group has been ascertained to correspond to a desired programming state, and in that

the control circuit causes the circuit for applying programming pulses to apply at least one additional programming pulse to those memory cells in the group whose programming state is not re-ascertained to correspond to a desired programming state.

19. (Original) The integrated circuit of claim 18, wherein the at least one electrically programmable semiconductor memory comprises at least one memory of type of at least one of EPROM, EEPROM, and Flash memory.